What is claimed is:

1. A thin film transistor comprising:

a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region;

wherein a depletion layer is formed between the channel region and the drain region; and

the width of the depletion layer and photoconductive current are in a proportional relationship, the photoconductive current generated when the channel region is irradiated with light, and the width of the depletion layer is equal to or less than a value obtained on the basis of the proportional relationship so that the photoconductive current falls within a range of specified permissible values.

2. A thin film transistor according to claim 1, wherein the relationship of expression (1)

$$(R+30)\cdot W < A \quad (1)$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region.

3. A thin film transistor according to claim 2, wherein the relationship of expression (2)

(2)

$$(R+30)\cdot W<1\times10^{3}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region.

4. A thin film transistor according to claim 3, wherein the channel width W of the channel region is 2 μm or less.

5. A thin film transistor according to claim 3, wherein the sheet resistance of the drain region is in the range of from 20 kΩ/□ to 100 kΩ/□.

6. A thin film transistor according to claim 4, wherein the sheet resistance of the drain region in the range of from 20 kΩ/□ to 100 kΩ/□.

7. A thin film transistor for use as a switching element of a liquid crystal display device, the thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region, wherein:

a low concentration impurity region having an impurity concentration less than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, and the length ΔL of the low concentration impurity region is 1.0 μm or less, the luminance of a backlight of the liquid crystal display device being 2000 (cd/m^2) or higher.

8. A thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being disposed on either side of the channel region and the low concentration impurity region being formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (3)

$$\Delta L > (W \cdot Vlc)/36 \quad (3)$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, and W (μm) is the channel width of the channel region.

9. A thin film transistor according to claim 8, wherein the relationship of expression (4)

$$\Delta L < 1.5 \cdot (W/L) \quad (4)$$

is satisfied, where L (μm) is the channel length of the channel region.

10. A thin film transistor according to claim 9, wherein the channel width W (μm) of the channel region is 2 μm or less.

11. A thin film transistor according to claim 9, wherein the sheet

resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

12. A thin film transistor according to claim 10, wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

13. A thin film transistor according to claim 11, wherein the low concentration impurity region is formed only in the region between the drain region and the channel region.

14. A liquid crystal display device comprising:

a liquid crystal panel portion comprising thin film transistors serving as switching elements, each of the thin film transistors being a thin film transistor of claim 1; and

a backlight portion for supplying light from a rear surface side of the liquid crystal panel portion;

wherein the relationship of expression (5)

$$(R+30)\cdot B\cdot W < C \tag{5}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region.

15. A liquid crystal display device according to claim 14, wherein the relationship of expression (6)

(6)

$$(R+30)\cdot B\cdot W<1\times10^{6}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region.

16. An EL display device comprising a light-emitting layer and a counter electrode formed thereon, the light-emitting layer being on a pixel electrode upper layer formed on a substrate having thin film transistors, the display device wherein:

each of the thin film transistors is a thin film transistor of claim 1, and the relationship of expression (5)

(5)

$$(R+30)\cdot B\cdot W<C$$

is satisfied, where B (cd/m^2) is the light intensity of light applied to a channel region of each of the thin film transistors.

17. An EL display device according to claim 16, wherein the relationship of the expression (6)

(6)

$$(R+30)\cdot B\cdot W<1\times10^{6}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the light intensity of light applied to the channel region, and W (μm) is the channel width of the channel region.

18. A method of producing a thin film transistor, comprising the steps

of:

forming a polycrystalline silicon semiconductor layer on an insulating substrate;

forming a gate insulating film on the polycrystalline silicon semiconductor layer;

forming a gate electrode in a pattern on the gate insulating film;

carrying out anodic oxidation by oxidizing a side surface of the gate electrode to form a metal oxide film covering the side surface of the gate electrode; and

doping the polycrystalline silicon semiconductor layer with impurities, the gate electrode being used as a mask;

wherein the thickness of the metal oxide film formed in the step of carrying out anodic oxidation is controlled to make the length ΔL of a low concentration impurity region formed in the step of carrying out impurity doping 1.0 μm or less.

19. A method of producing a thin film transistor, comprising the steps of:

forming a polycrystalline silicon semiconductor layer on an insulating substrate;

forming a gate insulating film on the polycrystalline silicon semiconductor layer;

forming a gate electrode in a pattern on the gate insulating film;

carrying out a first impurity doping by doping the polycrystalline silicon semiconductor layer with impurities, using the gate

electrode as a mask;

forming a masking film on a semiconductor region doped with impurities in the step of carrying out a first impurity doping, the masking film being formed in a pattern by anisotropic etching;

carrying out a second impurity doping by doping the polycrystalline silicon semiconductor layer with impurities using the masking film as a mask so that an impurity concentration difference exists between a region under the masking film and regions other than the region under the masking film, whereby a low concentration impurity region having an impurity concentration lower than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region and by making the length of the low concentration impurity region 1.0 μm or less.

20. A method of producing a thin film transistor according to claim 19, further comprising a step of inspecting by designating the thin film transistor having a low concentration impurity region with a length ΔL of 1.0 μm or less a quality product.